Operator's Manual

LeCroy

Innovators in Instrumentation

OPERATOR'S MANUAL

MODEL 8901A
CAMAC TO GPIB
INTERFACE

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LeCroy

Innovators in Instrumentation

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CAUTION

INSTALLATION

Crate power should be turned off during insertion or removal of modules to avoid possible damage caused by momentary misalignment of contacts.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

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1 GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation, packaged separately, should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in–warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Services Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977–6499, (914) 578–6059, or your local field service office.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on–site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state–of–the–art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up–to–date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

2 PRODUCT DESCRIPTION

GENERAL

The Model 8901A is a CAMAC module which provides GPIB access to a CAMAC mainframe.

CAMAC is an international standard for modularized instrumentation as defined by the ESONE Committee and the IEEE (Standard #583). Its function is to provide a means by which a wide range of modular instruments can be powered in a multi–receptacle crate and interfaced to a computer. The LeCroy Model 8901A CAMAC to GPIB (IEEE 488) interface allows the CAMAC system configuration to be used with GPIB computer controllers. For additional information on the IEEE 583 CAMAC standard, See Chapter 6.

Simple program instructions via the GPIB to registers in the Model 8901A select an individual instrument module within the CAMAC mainframe, select any subaddress within that module, and establish the function (read, write, control). This allows the user to handle the entire CAMAC mainframe of up to 23 individual instrument modules in the same manner as any ordinary single device connected to the IEEE–488 bus. It is possible to interconnect up to 15 different CAMAC mainframes in this way.

The 8901A can be programmed to do a block transfer of all data within a CAMAC module to a GPIB Listener without additional intermediate commands. In this mode, the 8901A will alternately transfer one, two or three 8–bit bytes (as programmed) as fast as the Listener can accept them (at rates approaching 500 kilobytes/sec) and then initiate a new CAMAC acquisition cycle.

The Model 8901A is a direct replacement for both the LeCroy Model 8901 and 8901/100 (Mod 100) and will work with LeCroy 6900 series CATALYST software. In addition to all of the 8901–8901/100 features, the "A" version includes the generation of the GPIB EOI signal at the end of valid data, a jumper to select the order in which data bytes are sent to the GPIB controller, and a "slow" block mode transfer for instruments that cannot be read out at full CAMAC speed.

SPECIFICATIONS

Internal Registers

Registers in the 8901A Interface are sequentially loaded with data after it has been commanded to enter the Listen mode by the GPIB System Controller. These registers store all the information necessary (F, A, N, W, C, Z, I) to generate standard CAMAC cycles.

The first byte received by the interface after it has entered the Listen mode contains either the CAMAC Function (F Code) or

control information. The second and sequential bytes accept, respectively, the CAMAC subaddress (A Code), station number (N Code) and three bytes of data for the CAMAC write lines.

Once these registers have been loaded, the information will be retained until modified or power is turned off. The GPIB system controller must issue a Listen command in order to initiate this loading procedure. The loading process can be terminated after any number of bytes have been transferred by issuing a Talk, Listen, Unlisten or IFC command.

CAMAC Cycles

A CAMAC cycle is executed every time the 8901A is commanded to enter the Talk mode and a Service Request is not pending. At the completion of the CAMAC cycle a DAV (Data Valid) will be asserted. Every time a byte is accepted a new byte is made available. When no more data is available, the 8901A asserts End of Identity (EOI).

Clear, Initialize and Inhibit

The 8901A can be programmed to generate clear (C), initialize (Z), or inhibit (I) signals on the dataway when a CAMAC cycle is executed. The C and Z registers are cleared after the completion of the next CAMAC cycle. The inhibit register will remain set until it is programmed off.

Block Transfer Mode

The 8901A can be programmed to do a high speed block transfer of 8–, 16–, or 24–bit words from CAMAC modules with read and increment capability. Following module addressing and the appropriate control byte, a Talk command will start the 8901A to read one, two, or three bytes of data and automatically initiate another CAMAC cycle. Approximately 2 μsec later (a programmable 40 μsec delay can be used for slow modules) new data is available to be read. CAMAC cycles will continue to be executed until a Q=0 (end of memory) condition causes the 8901A to stop executing CAMAC cycles and exit the transfer mode.

Service Requests (SRQ)

The 8901A will issue a Service Request when a LAM is set by a CAMAC module, or when a CAMAC cycle is executed and a Q=0 or X=0 response is detected.

Serial Poll

When the 8901A is polled, it sends up to five status bytes to the controller, terminating the Request after the controller reads the status byte. For a LAM–generated Service Request, the LAM must be cleared or disabled before the poll is taken, or else another service request will immediately be issued.

Front Panel LED's

Talk: indicates when 8901A is a Talker.
Listen: indicates when 8901A is a Listener.

Srq Enable: indicates when 8901A is enabled to carry out Service Requests.
X Response: indicates a valid command was accepted in the mainframe.
Q Response: indicates a valid data transfer or valid test within the mainframe.
Look–at–Me: indicates when any CAMAC modules sets "LAM" (a Service Request).
Inhibit: indicates when CAMAC dataway is inhibited.

GPIB Address Switch

Sets the GPIB Address of the 8901A

General

The 8901A resides in the two slots furthest right in a CAMAC mainframe and generates all CAMAC dataway signals in response to commands from a GPIB controller. A standard GPIB connector on the front panel permits interconnection to any GPIB system. This allows any GPIB controller to program settings, read from or write to any standard CAMAC modules.

Packaging: is in conformance with CAMAC standard, RF shielded #2 module.

Power Required: is 1.2 A at +6 V.

COMMANDS

Service Request (SRQ) Setup

Addressing the 8901A and presenting a setup byte determines the condition which generates an SRQ (Table 1).

Table 1 - SRQ Setup

SRQ Condition	Setup	Byte
LAM	65	(41)
Q=0	66	(42)
X=0	68	(44)
LAM or Q=0	67	(43)
LAM or X=0	69	(45)
Q=0 or X=0	70	(46)
LAM, Q=0 or X=0	71	(47)
Disable SRQ	64	(40)

Single byte commands – values specified in decimal with hex value given in ()

Transfer Mode

Addressing the 8901A and presenting a transfer byte determines the data transfer mode carried out with the subsequent execute (Talk) command (Table 2).

Table 2 – Transfer Mode Commands

	Normal Transfer	Block Read	High Speed Block Read
8-bit read	97 (61)	121 (79)	105 (69)
16-bit read	98 (62)	122 (7A)	106 (6A)
24-bit read	100 (64)	124 (7C)	108 (6C)

Single byte commands – values specified in decimal with hex value given in ()

Common CAMAC Commands

Addressing the 8901A and presenting it with the following byte determines a command which will be executed with the next Talk command (Table 3).

Table 3 – CAMAC Commands

Send initialize (Z)	33 (21)
Send clear (C)	34 (22)
Send clear and initialize	35 (23)
Assert inhibit (I)	72 (48)
Deassert inhibit (also disables SRQ's)	64 (40)

Single byte commands – values specified in decimal with hex value given in ()

Execute

Addressing the 8901A and presenting a TALK command executes the previously presented CAMAC command.

3 INSTALLATION

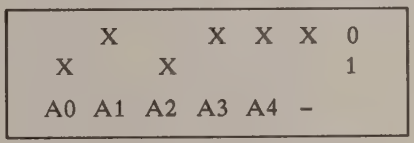
SETUP OF JUMPERS AND MECHANICAL SWITCHES

Before installation in a mainframe, it is desirable to set the GPIB and byte order jumpers as follows:

GPIB Address

Each device connected to the GPIB must have a unique address which the system controller uses to communicate with it. The address of the Model 8901A is set by a DIP switch located under the GPIB connector on the front panel. The switches are labeled A0,A1,A2,A3,A4 (representing values of 1,2,4,8,16 respectively). Valid GPIB address are 0 to 31. Figure 3.1 shows an address setting of 5 as an example.

GPIB Address Switch Settings



(X indicates switch depressed)

Figure 3.1

Byte Order Jumpers

On the side panel of the Model 8901A are two pair of jumpers labeled "NORMAL" and "REVERSE". These jumpers determine the order in which the data bytes are read out. When the jumpers are set to normal, the least significant byte of data is read out first in multibyte transfers. When in the reverse byte position, a 16-bit word is read out, most significant byte first, followed by the least significant byte. If 24-bit transfer is selected, the order is middle byte, least significant byte and then most significant byte. It is recommended that the reverse byte option only be used when the computer expects the MSB before the LSB in a 16-bit word. Caution – this jumper only controls the byte order for reading out of the 8901A. It does not effect the "write" data.

INSTALLATION IN MAINFRAME

The 8901A is compatible with any CAMAC mainframe.

With the power off, insert the 8901a into the Control Station location (the two rightmost locations in the mainframe).

Connect a GPIB cable from the 8901A to the GPIB interface associated with your computer.

Always ensure that the mainframe has sufficient clearance at the top to permit adequate airflow. During operation in the 8013A

benchtop instrument mainframe, air–blocking baffles (Models BFP–1 and BFP–2) should be used to ensure proper cooling. Do not obstruct ventilation by placing papers or other objects on the top of the mainframe.

4 OPERATING INSTRUCTIONS

INTRODUCTION

The 8901A provides GPIB control of all instruments in a CAMAC mainframe.

Waveform Catalyst

LeCroy WAVEFORM CATALYST system provides digital storage scope operation of one or more CAMAC mainframes using keystroke commands on a properly configured IBM PC or compatible. No programming of the 8901A is required in this instance. See WAVEFORM CATALYST Operator's Manual.

User Programming

The GPIB controller may send the 8901A two types of commands. The first type, setup commands, program the 8901A, while the second type, CAMAC commands, is used by the 8901A to program the operation of instruments in the mainframe.

SETUP COMMANDS

The setup commands are used to program the 8901A for the desired transfer mode, and SRQ (service request) response. All of these commands are single bytes; that is, the 8901A must first be addressed to Listen, followed by the command byte.

Transfer Mode Commands

By sending the appropriate command (see Table 1), the 8901A can be programmed to return 8, 16, or 24–bit data words in either single or block word transfers, whenever it executes a CAMAC cycle. In the case of multiple byte transfers, the least significant byte is sent first (if the byte jumpers are set to normal – see Chapter 3 for more details). A CAMAC cycle is executed every time the 8901A is addressed to Talk by the GPIB controller. In normal non–block mode, after the 1, 2, or 3 data bytes have been read, a status byte is sent containing the X response (least significant bit) and the Q response (bit 2) along with the GPIB EOI status line asserted to indicate that this is the end of the data to be transferred.

If a "block mode" read command had been sent, the 8901A will automatically initiate another CAMAC cycle when the GPIB controller has finished reading the current data word. CAMAC cycles will continue to be executed until Q = 0 or the GPIB controller terminates the transfer. There are two block modes in the 8901A. The first one, "block read" is provided for modules which cannot read out at full CAMAC speed (1 MHz). In this mode, a 35 µsec delay (plus GPIB overhead) is added between each CAMAC cycle to slow down the transfer rate. The other mode, "high speed block read" runs as fast as the data is read out over the GPIB, up to 2 µsec per cycle.

When block mode transfers are terminated normally (data read until Q=0) two additional bytes are sent to the GPIB controller. The first one is the status byte followed by a zero byte and EOI.

Note that in block mode transfers, since the 8901A is initiating the CAMAC cycles, if the GPIB controller terminates the transfer before Q=0, one additional cycle will be executed and the data will be left in the 8901A's registers. To access this data it is necessary to send the CAMAC command F(0), A(0), and N(24) (see next section) and then read out the data word. At the end of the block transfer, the 8901A is set to the corresponding normal transfer mode.

Table 1 – Transfer Mode Commands

	Normal Transfer	Block Read	High Speed Block Read
8–bit read	97 (61)	121 (79)	105 (69)
16–bit read	98 (62)	122 (7A)	106 (6A)
24–bit read	100 (64)	124 (7C)	108 (6C)

Single byte commands – values specified in decimal with hex value given in ()

Service Request Response Commands

A service request (SRQ) is a mechanism by which a GPIB compatible instrument can tell a computer that a particular condition exists, without the computer having to read a byte of information. There are three conditions occurring on the CAMAC bus which can cause the Model 8901A to issue a service request to the GPIB controller: When a LAM is set, and when Q and/or X indicate that invalid data/commands occurred during a transfer. Table 2 below lists the commands to send to the 8901A to set it up to generate a SRQ on the proper condition(s).

The GPIB controller must perform a serial poll of all devices after receiving a service request. When the 8901A is polled, it sends up to 5 bytes of information to the GPIB controller. The first byte is a status byte which contains the current state of X and Q in bits 1 (LSB) and 2 respectively and bit 7 indicating whether or not the currently addressed 8901A was the device which requested service. If bit 7 is equal to one, the 8901A generated the request. The next four bytes indicate the state of the LAM lines. They are encoded as follows:

LAM for slots 1 through 6 are in byte 2 (LAM 1 is LSB)

LAM for slots 7 through 12 are in byte 3

LAM for slots 13 through 18 are in byte 4

LAM for slots 19 through 23 are in byte 5

A service request by the 8901A will be cleared after the controller reads the status byte. However, if the request was caused by a LAM, a service request will immediately be issued again unless SRQ on LAM is disabled in the 8901A or the LAM is cleared in the instrument(s) asserting it. It is important to note that the 8901A cannot execute any CAMAC commands while any service request is pending.

Table 2 – Service Request Response Commands

Disable all SRQ's	64	(40)
Enable SRQ on occurrence of LAM	65	(41)
Enable SRQ on occurrence of Q=0	66	(42)
Enable SRQ on occurrence of X=0	68	(44)
Enable SRQ on occurrence of LAM or Q=0	67	(43)
Enable SRQ on occurrence of LAM or X=0	69	(45)
Enable SRQ on occurrence of Q=0 or X=0	70	(46)
Enable SRQ on occurrence of LAM, Q=0, or X=0	71	(47)

NOTE: All of these commands deassert inhibit

Single byte commands – values specified in decimal with hex value given in ()

PROGRAMMING CAMAC MODULES

Commands Common to All Instruments

The 8901A can be programmed to generate clear (C), initialize (Z), or inhibit (I) signals on the Dataway when a CAMAC cycle is executed. These commands operate on all instruments in the mainframe without any further addressing. The clear and initialize signals will be turned on only during the first CAMAC cycle executed after the 8901A received that command. The inhibit line will remain asserted until the 8901A is programmed to deassert it. *Caution – changing the inhibit line will affect the state of the service request response programming.*

Table 3 lists the 8901A commands to perform these functions.

Table 3 – CAMAC Commands

Send initialize (Z)	33	(21)
Send clear (C)	34	(22)
Send clear and initialize	35	(23)
Assert inhibit (I)	72	(48)
Deassert inhibit (also disables SRQ's)	64	(40)

Single byte commands – values specified in decimal

Commands to an Individual Instrument

To send a CAMAC command to a particular instrument the GPIB controller must address the 8901A to Listen and load it with the desired command information. If the first byte received by the interface after entering Listen mode is a valid CAMAC function (F) code, (0 to 31) the 8901A assumes that it is being sent a command sequence. The second byte expected is the CAMAC subaddress (A) code. This is followed by the CAMAC station number (N) code and up to three bytes of data (least significant byte first). Once the command is sent to the 8901A the information will be retained until modified or the power is turned off. The GPIB system computer may terminate the command loading procedure after any number of bytes have been sent. In other words, if the only difference between the last CAMAC command and the next one to be sent is the F code, it is not necessary to send a new A, N, etc.

After loading the 8901A with the desired command, a CAMAC cycle must be executed (by addressing the 8901A to Talk) to send the command to the particular instrument.

PROGRAMMING EXAMPLE

The following example illustrates the use of most of the 8901A commands. The procedure uses the following typical sequence of commands to control a LeCroy Model TR8837F Transient Recorder.

Initialize the instruments upon power on
Enable LAM
Initiate sampling
Wait for trigger
Enable TR8837 for reading
Read data out in high speed mode
Read acquisition parameters

The implementation of this sequence (from the GPIB system controller) is given below. The following notation is used:

OUT x,y,... indicates a transfer from the GPIB controller to the 8901A. It includes addressing the 8901A to Listen, sending the data byte(s) to it, and then sending the GPIB Unlisten command.

IN b1,...bn,r indicates a n+1 byte transfer from the 8901A to the GPIB controller (b1 ... bn are data bytes, r is the CAMAC response byte

with bits X and Q). It includes addressing the appropriate 8901A to Talk, reading the data byte(s) into the computer, and then sending the GPIB Untalk.

TALK — indicates sending out the GPIB Talk address to the specific 8901A. This is used to execute a CAMAC cycle when no data is to be returned. The "IN" command may be substituted if desired (e.g., to allow monitoring the CAMAC response bits X and Q).

For purposes of this example, assume that the Model 8901A is at GPIB address 1 and the Model TR8837F is in slot 3.

	GPIB bus transfers (bytes in decimal)
Initialize the Instruments	
Initialize the crate by sending CAMAC Z	OUT 33
Execute CAMAC cycle by addressing 8901A to Talk	TALK
Program instrument's parameters by sending F(16), A(0), N(3), d1, d2 (d1, d2 are the parameter settings – see TR8837F manual for details)	OUT 16,0,3,d1,d2
Program 8901A to return 8 bits of data and the CAMAC response byte	OUT 97
Execute CAMAC cycle and get CAMAC response	IN b1, r
Enable LAM	
Program 8901A to set SRQ on LAM	OUT 65
Enable TR8837F to generate LAM by sending F(26) (*note that since the A and N have not changed it is not necessary to resend them*)	OUT 26
Execute CAMAC cycle by addressing 8901A to Talk	TALK
Initiate Sampling	
Initiate sampling in the TR8837F with a F(9), A(0),N(3)	OUT 9,0,3
Execute CAMAC cycle by addressing 8901A to Talk	TALK
Wait for Trigger	
At this point, the TR8837F is waiting for a trigger (either external or from an F(25) sent to it). After the trigger occurs and the module is finished acquiring data, it will generate a service request.	
Perform a serial poll to determine which instrument set LAM (assuming there is more than one).	
Disable the 8901A from generating another SRQ	OUT 64
Send the GPIB serial poll enable command	SPE

Read in the 5 status bytes	IN r,L1,L2,L3,L4
Send the GPIB serial poll disable command	SPD

Enable TR8837F for Reading

Clear LAM in TR8837F with F(10),A(0),N(3)	OUT 10,0,3
Execute CAMAC cycle by addressing 8901A to Talk	TALK 1
Enable read mode in the TR8837F with an F(17), A(0),N(3)	OUT 17,0,3
Execute CAMAC cycle by addressing 8901A to Talk	TALK

Read Data

Set 8901A up for a high speed block read of 8-bit data words	OUT 105
Send F(2) to TR8837F – command to read data	OUT 2,0,3
Execute a CAMAC cycle and read all of the data out (at end of data, module sets Q to 0, the 8901A then sends the response byte followed by a 0 with the GPIB EOI bit set	IN b1,...,bn,r,0

Read Acquisition Parameters

Program the 8901A for a 16-bit data word	OUT 98
Tell the TR8837F to send its parameters (F(0),A(0),N(0))	OUT 0,0,3
Execute CAMAC cycle and get 2 bytes containing its acquisition parameters and the CAMAC response byte	IN b1,b2,r

The following are working examples of programming the LeCroy Model TR8828C 200 megasample/sec or TR8818 100 megasample/sec modular recorders using the Model 8901A and the HP9836 desktop computer. HP BASIC Version 3.0 was used for writing the code. Additional and complete function commands for the digitizers and 8901A interface are contained in the respective manuals.

Highlights of 8901A and Digitizer Programming:

The 8901A was set to a device address of 1 and called from HP code as device 701, as shown below:

OUTPUT 701 USING "#, B"; 17, 0, 8

The "#, B" sets the format of data as BINARY. In this example, the F=17 command A=0, N=slot 8 sets the data pointer back to the beginning of memory prior to reading out memory.

Sending a command to a digitizer is done the CAMO subroutine, lines 10000 to 10091. Note that upon programming a

module, a talk byte (line 10080) is sent to the 8901a to initiate a cycle in the instrument mainframe. Function code, sub address, slot and bytes are predefined for setup, arming, triggering, and reading setting setting memory pointer to beginning. Upon entering the CAMO subroutine the bytes are sent over the GPIB. Figure 1 illustrates the sequence of operations used to program a recorder. Upon filling memory, a LAM (Look-At-Me) flag is initiated to the 8901A for the digitizer slot. A service request (SRQ) is sent to the HP9836. A Serial Poll Service Subroutine (lines 10100 to 10190) is initiated to handle the SRQ, read 5 Status Bytes from the 8901A, and clear the LAM.

Data transfer is programmed in lines 10400 to 10419. Note that since the TR8818 and TR8828C send out 2 bytes in the mainframe, lines 10420 to 10449 are used to restore data and convert data to integers, that can be plotted on the computer screen.

In addition to programming modules using F-A-N commands in the CAMO section, decimal bytes are used to program the 8901A module for the form of data to send over the bus. For example, line 10413 programs the 8901A module for high speed block reads of data by transmitting byte 106. When in block read mode a single Function Command of 2 sent to the digitizer initiates a data read from the recorder until memory has been depleted.

The same output subroutine used for digitizers is used to program other LeCroy modules, such as a signal conditioner, clock generator module, or gate and delay generator. The set of function commands defined for each module are inserted to obtain the desired state of operation.

A detailed listing of the above program follows along with comments explaining each subroutine and statement.

```
10      ! TR8K_16ST:
11      !
14      !*********************************************************************
15      !              THIS PROGRAM READS OUT A TR8828 USING AN 8K "TRANSFER"
16      !              IN HIGH SPEED BLOCK READ MODE 16 BIT TRANSFERS
17      ! ***********  EACH POINT IS READ INTO A STRING VARIABLE ***********
18      ! ***********  THEN CONVERTED TO AN INTEGER ****************
19      !*********************************************************************
30      !
31      ON KBD GOSUB Ggrid
32      Flag=1                                          !GRID ON OFF FLAG
34      ASSIGN @GPIB TO 701
35      !
40      PRINT CHR$(12)                                  !CLEAR SCREEN
41      GCLEAR
43      CLEAR 7                                         !CLEAR GPIB
44      CLEAR 701
50      !
60      PRINT "         Sampling Period"
70      PRINT"-------------------------------------------------------------------------"
80      PRINT "         1 = 5 ns                5 = 80 ns"
90      PRINT "         2 = 10 ns               6 = 160 ns"
100     PRINT "         3 = 20 ns               7 = 320 ns"
110     PRINT "         4 = 40 ns               8 = EXT CLK"
120     !
130     PRINT
140     PRINT
150     INTEGER Pretrig                         !DECLARE INTEGER
160     INTEGER N,F,A,Dat1,Dat2,Mask
161     A=0
170     !
180     INPUT "ENTER SLOT NUMBER",N             !GET SLOT NUMBER
190     INPUT "ENTER SAMPLING PERIOD : ",Clk    !GET SAMPLE CLOCK
200     IF Clk<1 THEN 190
210     IF Clk>8 THEN 190
220     PRINT
230     INPUT " ENTER n/8 PRE-TRIGGER SAMPLES: ",Pretrig
240     IF Pretrig<0 THEN 230
250     IF Pretrig>8 THEN 230
251     INPUT "A(uto) or E(xternal) STOP TRIGGER ? :",Mode$
253     !
254     OUTPUT 701 USING "#,B";33               !SEND Z TO INITIALIZE CRATE
255     !
256     Clk=Clk-1
258     Dat1=Pretrig+(Clk*16)
259     Dat2=0                                  !SET UP CONTROL WORD (FIXED 16K MEMORY SIZE)
261     F=16
264     GOSUB Camo                              !WRITE OUT CONTROL WORD
265     !
266     Start:
267     !
268     !
269     !
270     F=10
271     GOSUB Camo                              !CLEAR LAM
272     F=24
273     GOSUB Camo                              !DISABLE LAM
```

```
274     !
276     !
277     F=19
278     Dat1=128
279     GOSUB Camo                          !WRITE OUT ZERO INPUT OFFSET
280     !
283     F=26                                !ENABLE LAM
286     GOSUB Camo
287     !
289     F=9                                 !START DIGITIZER
290     GOSUB Camo
292     !
293     !
294     IF Mode="A" THEN Trig               !IF "A" THEN ISSUE STOP TRIGGER
295     GOTO 301
296 Trig:                                  !
297     F=25
295     GOTO 301
296 Trig:
297     F=25
298     GOSUB Camo                          !SEND COMPUTER STOP TRIGGER
299     !
301     OUTPUT 701 USING "#,B";65           !ENABLE SRQ
302     !
303     ON INTR 7 GOTO Getdata !Serpol      !ENABLE INTERUPT
304     ENABLE INTR 7;2
305     GOTO 305                            !SIT AND WAIT FOR INTERRUPT
306     !
307 Getdata;                               !
308     GOSUB Serpol                        !GO TO SERIAL POLL SUBROUTINE
309     GOSUB Trans8k                       !GO READ DATA WITH A "TRANSFER"
310     GOTO Plot8k                         ! GO PLOT DATA
+01     !+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
10010   !***************************************************************************
10020   !                          SUBROUTINES ( CAMO ), ( SERPOL )
10030   !
10031   !              CAMAC OUTPUT SUBROUTINE --- SERIAL POLL SERVICE SUBROUTINE
10040   !***************************************************************************
10050   !
10060   Camo;! SUBROUTINE CAMO
10070   OUTPUT 701 USING "#,B";F,A,N,Dat1,Dat2
10080   SEND 7; TALK 1 !TELL 8901 TO TALK
10090   RETURN
10091   !*************************************************************************
10100   !
10110   !
10120   Serpol; ! SERIAL POLL ROUTINE  RETURNS STATUS OF CRATE
10130   ! at this point SRQ WILL HAVE BEEN ASSERTED
10140   !
10141   DISABLE INTR 7                                          !DISABLE INTERRUPTS
10143   INTEGER Stat1,Stat2,Stat3,Stat4,Stat5
10150   OUTPUT 701 USING "#,B";64                               !DISABLE ANY FURTHER
                                                                 SRQ´S
10160   SEND Z;UNL MLA TALK 1 CMD 24                            !CONFIGURE BUS AND
                                                                 SEND SPE
10170   ENTER 7 USING "#,B"; Stat1,Stat2,Stat3,Stat4,Stat5      !GET STATUS
10180   SEND 7:CMD 25 UNT
```

```
10190   RETURN
10191   !
10192   !
10194   !*************************************************************************
10204   !
10390   !+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
10400   Trans8k:        !THIS SUBROUTINE WILL ACQUIRE 8K OF DATA USING A "TRANSFER"
        STATEMENT IN HIGH SPEED BLOCK TRANSFER MODE 16 BIT READS
10401   !+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
10402   !
10403   !
10405   INTEGER Datbuf(8192) BUFFER
10406   DIM Tempbuf$[8192]BUFFER                        !READ DATA 8 BITS AT A TIME
                                                         INTO STRING VARIABLE
10407   !
10408   ASSIGN @Buff TO BUFFER Tempbuf$;FORMAT OFF      ! DEFINE AN 8K BUFFER
10409   !
10410   F=17
10411   GOSUB Camo                                      !RESET READ POINTER
10412   !
10413   OUTPUT 701 USING "#,B";106                      !SET UP FOR HIGH SPEED BLOCK READ
10414   OUTPUT 701 USING "#,B",2,0,N                    !SEND OUT FIRST F2 COMMAND
10415   !
10416   TRANSFER @GPIB TO @Buff;END,WAIT                !TRANSFER 8K OF DATA
10417   !
10418   ASSIGN @Buff TO *
10419   !
10420   !!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
10421   !              RESTORE DATA TO 8 BIT BYTES AND PUT IN Datbuf IN CORRECT ORDER
10422   !
10423   !!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
10426   !
10427   FOR Fix=1 TO 6192
10430   Datbuf(Fix)=NUM( Tempbuf$[Fix])            !CONVERT STRONG ELEMENTS TO INTEGER
10436   NEXT Fix
10439   !
10440   !
10441   !               SCALE DATA FOR PLOT
10442   !            ----------------------
10444   !
10445   FOR D=1 TO 8192
10446   Datbuf(D)=Datbuf(D)*2-256
10447   NEXT D
10448   !
10449   RETURN
10450   !
10451   !
10452   !
10453   Garid:                      !TURN GRID ON AND OFF
10454   Keys$=KBD$
10455   IF Keys$<>"G" THEN RETURN
10456   Gron=Gron EXOR Flag
10457   RETURN
10458   !
10459   !
30130   !*******************************************************
30140   !   PLOT 8K OF DATA
```

```
30150  !*****************************************************
30160  !
30161  !                                          !SUBROUTINE PLOT 8K
30173  PRINT CHR#(12)                        !CLEAR SCREEN
30180  GINIT
30190  GRAPHICS ON
30200  CSIZE 4
30210  MOVE 0,65
30220  Label1$="AMPLITUDE"
30230  FOR L=1 TO 9
30240  LABEL Label$[L,L]
30250  NEXT L
30260  !
30270  MOVE 43,0
30280  LABEL  "NUMBER OF SAMPLES"           !LABEL X AXES
30290  !
30300  VIEWPOINT 15,125,15,90
30310  WINDOW 0,8192,-256,256
30320  AXES 1024,64,0,-255
30321  AXES 1024,64,8192,255
30322  !
30323  IF Gron=0 THEN 30327                 !CHECK GRIP ON OFF FLAG IF ZERO TURN OFF
30324  !
30326  GRID 102+,6+,0,-255
30327  CLIP OFF
30328  CSIZE 4
30329  LORG 8
30330  FOR Ylab=-256 TO 256 STEP 64
30331  MOVE -1,Ylab
30332  LABEL USING "#,K";Ylab               !LABEL Y AXIS
30333  NEXT Ylab
30334  Xlab=1024
30335  !
30336  FOR Xax=1350 TO 8518 STEP 1024
30337  MOVE Xax,-280
30338  LABEL USING "#,K";Xlab
30339  Xlab=Xlab+1024
30340  NEXT Xax
30342  !
30343  IF Datbuf(1)=0 THEN Bufpoint=16
30344  IF Datbuf(1)>0 THEN Bufpoint=17              !SET UP BUFFER POINTER
30345  !
30347  FOR P=Bufpoint TO 8192               !DUMP FIRST AND LAST 16 POINTS
30350  PLOT P,Datbuf(P),1
30360  NEXT P
30361  SEND 7;UNT
30363  CLEAR 7
30368  GOTO Start
30370  END
```

5 THEORY OF OPERATION

GENERAL

The Model 8901A is a GPIB to CAMAC interface which is composed of two circuit boards. The first board plugs into the control (rightmost) slot of the CAMAC mainframe and interfaces to the CAMAC station number (N) lines and LAM lines. This board also contains the GPIB interface circuitry. The second board provides the interface to the CAMAC Dataway. It has registers to store the CAMAC commands sent by the GPIB controller and drive the function (F), address (A), and write data (W) lines of the Dataway during a CAMAC cycle. It also has the circuit to generate the CAMAC cycle timing and latch the read data (R) lines.

The 8901A circuitry can be broken down into logical subsections as shown in the block diagram. The operation of each of these subsections is discussed below.

GPIB COMMAND DECODER

At the heart of the 8901A is the GPIB command decoder. When a command is put on the GPIB bus it must be interpreted by the 8901A and a decision must be made as to how (if at all) to respond to it. The 8901A will respond to any of the following GPIB commands: interface clear (IFC), serial poll enable (SPE), serial poll disable (SPD), my Talk address (MTA), my Listen address (MLA), Unlisten (UNL), and Untalk (UNT).

The 8901A has four basic states: Idle, Talk mode, Listen mode, Serial poll mode. These states are entered and exited as a result of one of the above GPIB commands. The following table lists each of the commands and describes its effect on the 8901A's state.

IFC: Resets all registers in the 8901A and places it in the Idle state regardless of its current state.

SPE: Causes the 8901A to enter Serial Poll mode.

SPD: If the 8901A is in Serial Poll mode, this command returns it to the Idle state. It also clears a pending service request (SRQ).

MTA: If in Serial Poll mode, the 8901A will output its SRQ status upon receiving its Talk address. If not in Serial Poll mode, receipt of MTA will cause a CAMAC cycle to be executed and Talk mode to be entered.

UNT: Takes the 8901A out of Talk mode if it is active MLA – Causes the 8901A to enter Listen mode so that it may accept CAMAC or setup commands.

UNL: Places the 8901A into the Idle state if currently in Listen mode.

ACCEPTOR HANDSHAKE

The GPIB protocol provides a handshake for all data transfers. When a GPIB command is sent or the 8901A is in Listen mode, the 8901A must indicate that it is ready to receive a transfer by asserting the RFD line. The GPIB controller must then assert DAV when valid data is on the bus. The 8901A can then read in the data. It then asserts the DAC line to say the transfer is complete.

LISTEN MODE

Bits 6 and 7 of the first byte the 8901A receives from the GPIB Talker after entering Listen mode is used to determine whether the byte is a command for the 8901A itself, a "global" CAMAC command or a CAMAC command for a specific module. Bits 1–5 are then latched in the appropriate registers. If it's a CAMAC F command for a particular instrument, a sequencer is used to latch additional bytes in the following order: A, N, W1–8, W9–16, W10–24.

GLOBAL CAMAC COMMANDS

There are three global CAMAC commands: C, Z, and I. For each of these commands there is a corresponding line on the CAMAC Dataway which is driven by the 8901A whenever a CAMAC cycle is executed. The command is asserted if its latched value is a 1. At the end of the CAMAC cycle the C and Z latch is reset to zero.

F, A, N CAMAC COMMANDS

As described above, the values for F, A, N, and the Write data are latched when the information is sent from the GPIB controller. When a CAMAC cycle is executed, all of these lines are driven for the entire length of the cycle (while Busy is asserted). The latched values will not change until they are overwritten by a new command from the GPIB controller.

TRANSFER MODE

The commands for the 8901A determine how many bytes are to be read back, whether a new CAMAC cycle should be executed when data is read out (block mode), and what conditions (if any) should cause SRQ to be asserted by the 8901A. The latches for this information are cleared if an IFC is sent. The block transfer enable flip flop also is cleared when a Q = 0 is read in.

SERIAL POLL MODE

Serial poll is used by the GPIB controller to determine which device asserted SRQ. Upon decoding the serial poll enable command, the SPAS flip flop is set true, putting the 8901A in serial poll mode. When the controller then addresses the 8901A to Talk, the serial poll status bytes are sent instead of

data and CAMAC cycles are inhibited. Bit 7 of the status bytes indicates the state of the SRQ line while bits 1–6 are used for data. The first byte contains X and Q, while the next 4 bytes contain the LAM status (six slots/byte) starting with slot 1. The SRQ is cleared when all of the status is read out or when the 8901A receives a serial poll disable command.

TALK MODE

When the 8901A is addressed to Talk (and serial poll mode is not active) two things occur. First, the 8901A enters the Talker active state. This causes the direction of the GPIB buffers to be reversed, since the 8901A must now drive the GPIB bus and it must disable the acceptor handshake circuit and enable the source handshake circuit. Secondly, the 8901A starts the execution of a CAMAC cycle. Upon completion of the cycle the appropriate number of data bytes are sent to the GPIB Listener followed by the X and Q response byte which is sent with the EOI signal asserted.

SOURCE HANDSHAKE

Since the 8901A is in Talk mode, the GPIB handshaking protocol reverses. That is, the 8901A is now the one to indicate when data is valid. Three conditions must be met before it can assert DAV. First, it must be in Talk mode and ATN must be set false by the GPIB controller. Also it must wait for the GPIB controller (or Listener) to assert RFD. The last condition is that the CAMAC data must be latched into the 8901A during the CAMAC cycle. When all of these conditions have been met, the 8901A waits an additional 200 nsecs before asserting DAV to allow time for the data to become stable on the GPIB bus. When the listening device asserts DAC, DAV is cleared and a sequencer is clocked to output the next byte. This byte may be another data byte, or a status byte. If in block mode the status byte is suppressed, and a new CAMAC cycle is initiated instead.

CAMAC CYCLE TIMING

The CAMAC cycle starts when the 8901A is addressed to Talk or, if it is in block mode transfer, when the last data byte is read out. The 8901A asserts the Busy line and enables the F,A,N,W,C,Z and I drivers. Approximately 500 nsecs later, S1 is asserted for 250 nsecs. At the end of S1, all 24 bits of the CAMAC data lines, X, and Q are latched in the 8901A. S2 is asserted 125 nsecs later for 250 nsecs. The cycle is terminated 125 nsecs after S2 goes away, Busy is cleared and all drivers are disabled.

READ DATA

The sequencer described above determines which data byte is to read out. The order of the first two bytes may be reversed by

side–panel jumpers. The data is latched in the 8901A on every CAMAC cycle and generally read out immediately after the cycle completes. However, a special command (F(0), A(0), N(24)) is provided to allow readout of the latched data (the CAMAC cycle is inhibited) at a later time.

X AND Q RESPONSE

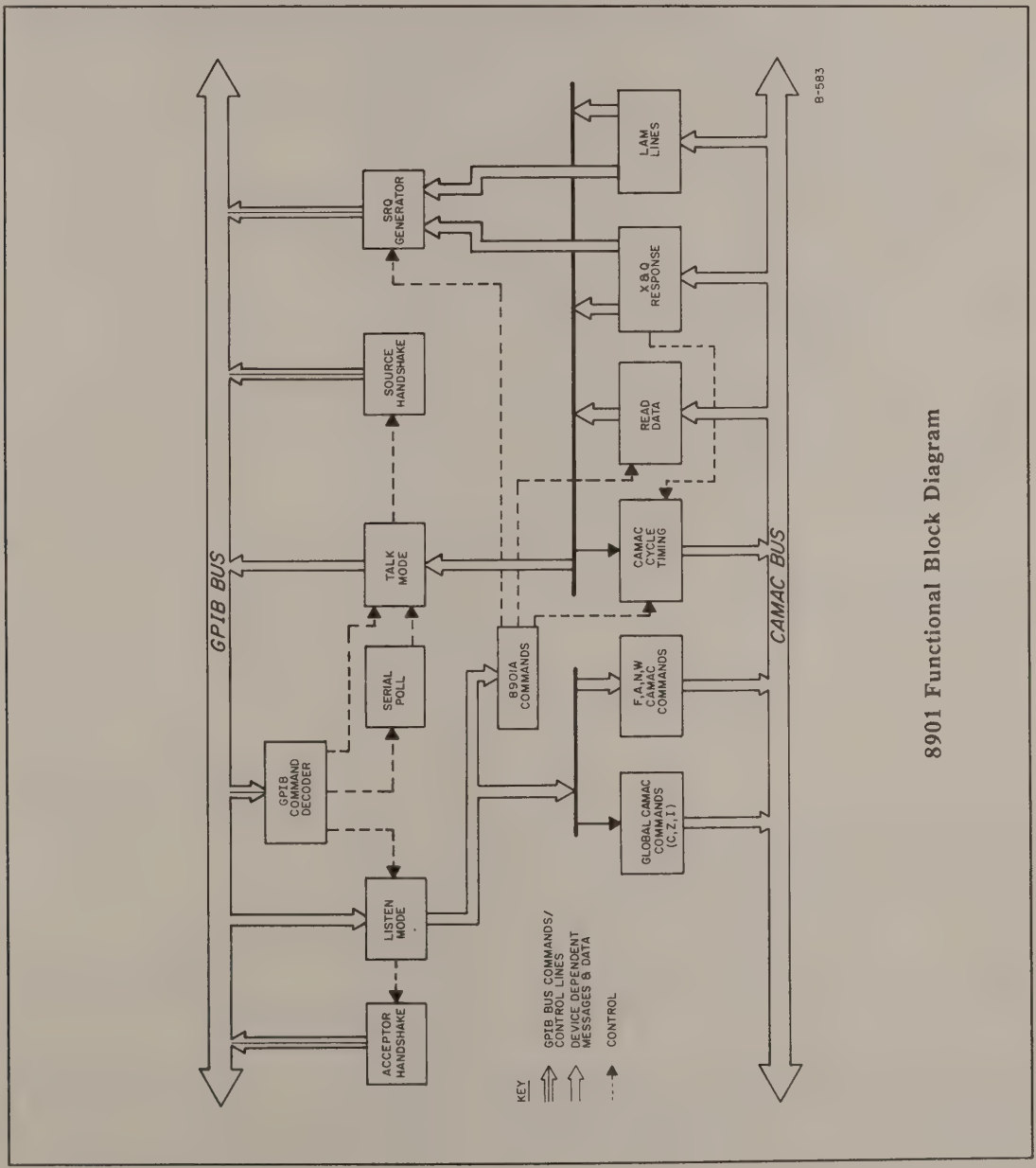
The X and Q responses are latched in the 8901A during the CAMAC cycle and read out in the response byte. They are also used in the generation of SRQ's and termination of block mode transfers.

LAM LINES

The LAM lines are used by the SRQ generation circuit and can be read by the GPIB controller when it's conducting a serial poll.

SRQ GENERATION

A service request (SRQ) may be generated (depending on how the 8901A is programmed) on any of the following conditions: a LAM is set by one of the CAMAC instruments, or a X = 0 or Q =0 response is detected during the execution of a CAMAC cycle. When a service request is pending, CAMAC cycles are inhibited until a serial poll is performed and the SRQ cleared. However, if the SRQ was caused by a LAM, unless the LAM is cleared or the 8901A is disabled to generate SRQ's on LAM before the serial poll is taken, another SRQ will be issued immediately.



8901 Functional Block Diagram

6 ADDITIONAL INFORMATION

DESCRIPTION OF CAMAC

CAMAC modules may be plugged into a CAMAC mainframe (called Crate in the CAMAC standard) which has up to 25 stations numbered 1 through 25. A station is a slot which accepts a CAMAC module. Some modules occupy several stations. The rightmost two stations are reserved for a Crate Interface or Controller whereas the remainder are Normal Stations used for instrumentation modules. The purpose of the crate controller is to issue CAMAC commands to the modules and transfer information between a computer and the CAMAC modules. It is the interface between the CAMAC Dataway and a computer.

All CAMAC operations take place over the CAMAC Dataway. The Dataway is a parallel bus used to transfer all data, the function coding information, and all status information. In a typical Dataway operation, the crate controller issues a CAMAC command which includes specifying a station number (N), a subaddress (A), and function code (F). In response, the module will generate a valid command accepted (X response) and act on the command. If this command requires data transfer, the read (R) or write (W) lines will be used. Note that the terms Read and Write apply to the crate controller, not the module. For example, under a read command, the crate controller reads data contained within a module.

Whenever there is no Dataway operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look–at–Me line to indicate that it requires attention.

There are also three common control signals made available at all stations:(Z) to Initialize all units, (C) to clear data registers, and (I) to Inhibit (e.g., data–taking).

Definition of CAMAC Commands

The CAMAC command consists of signals on the Dataway lines which specify at least one module (by individual station number lines), a subsection of the module or modules (by the four subaddress bus lines, and the function to be performed (by the five function bus lines). The command signals are maintained for the full duration of the operation on the Dataway.

Station Number

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station.

Subaddress Codes

Different sections of a module are addressed by signals on four A bus lines. These signals are decoded in the module to select one of up to 16 subaddresses, numbered in decimal from A(0) to A(15).

Function Codes

The function to be performed at the specified subaddress in the selected module or modules is defined by the signals on the five F bus lines (F16, F8, F4, F2, F1). These signals are decided in the module to select one of up to 32 functions, numbered in decimal from F(0) to F(31). To see to which functions a particular LeCroy instrument reacts, see its manual.

CAMAC Data

A common parallel highway is used for all data transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines

The crate controller generates data signals on the 24 parallel W bus lines (W1–W24) at the beginning of any Write operation.

The Read Lines

Data signals are set up on the 24 parallel R bus lines (R1–R24) by the instrumentation module as soon as a Read command is recognized. An interface such as the 8901A strobes data from the R bus lines into its own internal registers, whereafter the data is appropriately formatted for GPIB compatible transfers.

Status Information

CAMAC status information is conveyed by signals on the LAM, Busy (B), Response (Q) and Command Accepted (X) lines. This status information is similar to the GPIB service request.

Look–at–Me (LAM)

This, like the N Line, is an individual connection from each station to a separate pin at the control station. When there is no Dataway operation in progress (no B present) any plug–in unit may generate a signal on its L line to indicate that it requires attention, such as is the case when a waveform recorder has finished a conversion sequence. A LAM request can be reset by Clear LAM, Initialize, or by the performance of the specific action which generated the request.

Q Response

The Q busline is used during a Dataway operation to transmit a signal indicating the status of a selected feature of the module, such as whether or not data being read is valid.

Command Accepted

Whenever a module is addressed during a command operation it must generate an X=1 on the Command Accepted busline (X) if it recognizes the command as one that it is equipped to perform.

Command Controls and Signals

The following common control signals operate on all modules within the crate, without requiring address by a command.

Initialize

The initialize signal (Z) has absolute priority over all other signals or controls. It sets all units to a basic state by resetting all registers, and by resetting all LAM signals and disabling them where possible.

Inhibit

The presence of this signal (I) can be used by a module to inhibit any activity (for example, data-taking).

Clear

The common clear signal (C) resets all registers and bistables connected to it.

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